CLAIMS

We claim:

1. A memory system, comprising:

a first buffer mounted on a motherboard;

at least one first memory device coupled to the first buffer and mounted to the motherboard; and

a plurality of signal traces routed on the motherboard to the first buffer and the at least one first memory device.

2. The memory system of claim 1 where the first buffer is a command and address buffer capable of driving the at least one first memory device with address and command signals.

3. The memory system of claim 2 where the command and address buffer receives a command and address signal through a first command and address signal trace routed on the motherboard.

4. The memory system of claim 3

where the at least one first memory device receives the command and address signals outputted from the command and address buffer through a second command and address signal trace routed on the motherboard; and

where the first command and address signal trace is arranged substantially perpendicularly with the second command and address signal trace.

5. The memory system of claim 1 where the at least one first memory device is one of a DRAM and SDRAM.

6. The memory system of claim 1 where the at least one first memory device receives a data signal and a clock signal through corresponding data and clock signal traces routed on the motherboard.

7. The memory system of claim 1 comprising at least one memory module electrically coupled to a memory controller through a socket mounted on the motherboard.

8. The memory system of claim 7 where the at least one memory module comprises:

a second buffer mounted on a module board of the at least one memory module; and

at least one second memory device mounted on the module board of at least one memory module and coupled to the second buffer.

9. The memory system of claim 8 where the at least one second memory device is one of a DRAM and SDRAM.

10. The memory system of claim 7 where the at least one memory module is located farther from the memory controller on the motherboard than the at least one first memory device.

11. The memory system of claim 1 comprising a phase locked loop mounted on the motherboard and capable of generating a first clock signal on a second clock trace responsive to the system clock signal on a first clock trace, where the at least one first memory device is synchronous with the first clock signal.

12. The memory system of claim 1 comprising a delay locked loop mounted on the motherboard and capable of generating a first clock signal on a second clock trace responsive to the system clock signal on a first clock trace, where the at least one first memory device is operated in synchronization with the first clock signal.

13. The memory system of claim 11 where the first clock trace for the system clock is arranged substantially perpendicularly with the second clock trace for the first clock.

14. The memory system of claim 12 where the first clock trace for the system clock is arranged substantially perpendicularly with the second clock trace for the first clock.

15. A memory system, comprising:

at least one memory rank mounted directly on a motherboard; and

a plurality of signal traces routed on the motherboard to the at least one memory rank.

16. The memory system of claim 15 where the at least one memory rank comprises:

at least one first memory device; and

a first buffer capable of driving address and command signals to the at least one first memory device through corresponding signal traces routed on the motherboard.

17. The memory system of claim 16 where the at least one first buffer receives a command and address signal through a first command and address signal trace routed on the motherboard.

18. The memory system of claim 17

where the at least one first memory device receives the command and address signal outputted from the at least one first buffer through a second command and address signal trace routed on the motherboard; and

where the first command and address signal trace is arranged substantially perpendicularly with the second command and address signal trace

19. The memory system of claim 17 where the at least one first memory device receives a data signal and a clock signal through corresponding data and clock signal traces routed on the motherboard.

20. The memory system of claim 17 where the at least one first memory device is one of a DRAM and SDRAM.

21. The memory system of claim 20 comprising a phase locked loop capable of generating a first clock signal on a second clock trace responsive to a system clock signal on a first clock trace, where the at least one first memory device is operated in synchronization with the first clock signal.

22. The memory system of claim 20 comprising a delay locked loop capable of generating a first clock signal on a second clock trace responsive to a system clock signal on a first clock trace, where the at least one first memory device is synchronous with the first clock signal.

23. The memory system of claim 21 where the first clock trace for the system clock signal is arranged substantially perpendicularly with the second clock trace for the first clock signal.

24. The memory system of claim 22 where the first clock trace for the system clock signal is arranged substantially perpendicularly with the second clock trace for the first clock signal.

25. The memory system of claim 18 comprising:

a memory module; and

a receptacle mounted on the motherboard and capable of receiving the memory module.

26. The memory system of claim 25 where the memory module includes:

a plurality of second memory devices mounted on a module board of the memory module; and

a second buffer mounted on the module board of the memory module and capable of driving the plurality of second memory devices.

27. The memory system of claim 25 comprising a phase locked loop capable of generating a first clock responsive to a system clock, where the plurality of second memory devices are operated in synchronization with the first clock.

28. The memory system of claim 25 comprising a delay locked loop capable of generating a first clock responsive to a system clock, where the plurality of second memory devices are operated in synchronization with the first clock signal.

29. The memory system of claim 25 where the receptacle is located farther from a memory controller on the motherboard than the at least one first memory device.

30. A method comprising:

mounting a plurality of first memory devices on a motherboard; and

mounting a first command and address buffer capable of driving the plurality of memory devices on the motherboard with corresponding command and address signals.

31. The method of claim 30 comprising routing a first signal traces for the command and address signals from the buffer to the memory device on the motherboard.

32. The method of claim 31 comprising routing a second signal traces for the command and address signals from a memory controller mounted on the motherboard to the first command and address buffer, where the first signal traces is substantially perpendicular with the second signal traces.

33. The method of claim 31 comprising mounting a phase locked loop on the motherboard, the phase locked loop being capable of generating a first clock responsive to the system clock.

34. The method of claim 31 comprising mounting a delay locked loop on the motherboard, the delay locked loop being capable of generating a first clock responsive to the system clock.

35. The method of claim 31 comprising electrically coupling a memory module to a memory controller mounted on the motherboard through a receptacle mounted on the motherboard.

36. The method of claim 31 comprising:

mounting a second memory device on a module board of a memory module ; and

mounting a second command and address buffer on the module board, where the module board is coupled to a memory controller through a socket mounted on the motherboard .

37. The method of claim 36 comprising mounting a phase locked loop on the motherboard, the phase locked loop being capable of generating a first clock responsive to the system clock.

38. The method of claim 37 comprising mounting a delay locked loop on the motherboard, the delay locked loop being capable of generating a first clock responsive to the system clock.

39. A memory system, comprising:

a memory controller mounted directly on a motherboard and generating a plurality of command and address signals;

a first buffer mounted directly on the motherboard and receiving the command and address signals;

at least one first memory device coupled to the first buffer and mounted directly to the motherboard; and

a plurality of signal traces routed on the motherboard to the first buffer and the at least one first memory device.

40. A memory system, comprising:

a memory controller mounted directly on a motherboard and generating a plurality of command and address signals;

a first buffer mounted directly on the motherboard and receiving the command and address signals;

at least one first memory device coupled to the first buffer and mounted directly to the motherboard;

at least one memory module comprising a second buffer mounted on a module board and receiving the command and address signals, and at least one second memory device coupled to the second buffer, the at least one second memory device being mounted on farther from the memory controller than the the at least one first memory device;

a plurality of first signal traces routed on the motherboard to the first buffer and the at least one first memory device; and

a plurality of second signal traces routed on the module board to the second buffer and the at least one second memory device.

41. A memory system, comprising:

a memory controller mounted directly on a motherboard and generating a plurality of command and address signals

a first buffer mounted directly on the motherboard and receiving the command and address signals;

a phase locked loop mounted directly on the motherboard and receiving a clock signal;

at least one first memory device coupled to the first buffer and mounted directly to the motherboard; and

a plurality of signal traces routed on the motherboard to the first buffer and the at least one first memory device;

where the first memory device is synchronous with an internal clock signal outputted from the phase locked loop.

42. A memory system, comprising:

a memory controller mounted directly on a motherboard and generating a plurality of command and address signals;

a first buffer mounted directly on the motherboard and receiving the command and address signals;

a first phase locked loop mounted directly on the motherboard and receiving a clock signal;

at least one first memory device coupled to the first buffer and mounted directly to the motherboard;

at least one memory module comprising a second buffer mounted on a module board and receiving the command and address signals, and at least one second memory device coupled to the second buffer, the at least one second memory device being mounted on the motherboard farther from the memory controller than the at least one first memory device;

a second phase locked loop mounted on the module board and receiving the clock signal;

a plurality of first signal traces routed on the motherboard to the first buffer and the at least one first memory device; and

a plurality of second signal traces routed on the module board to the second buffer and the at least one second memory device;

where the first memory device operates synchronous with a first internal clock signal outputted from the first phase locked loop, the second memory device operates synchronous with a second internal clock signal outputted from the second phase locked loop.